How to use high bit-rates in a CAN-system with CAN-FD/EF

Presentation at ICC
11-12 2013 in Paris

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The test and verification Hardware

- Altera Cyclone IV FPGA, with 15k logic elements.
- FPGA includes PCI-express physical layer.
- 4 CAN-channels CAN/CAN-FD/CAN-EF.
- Galvanic isolation

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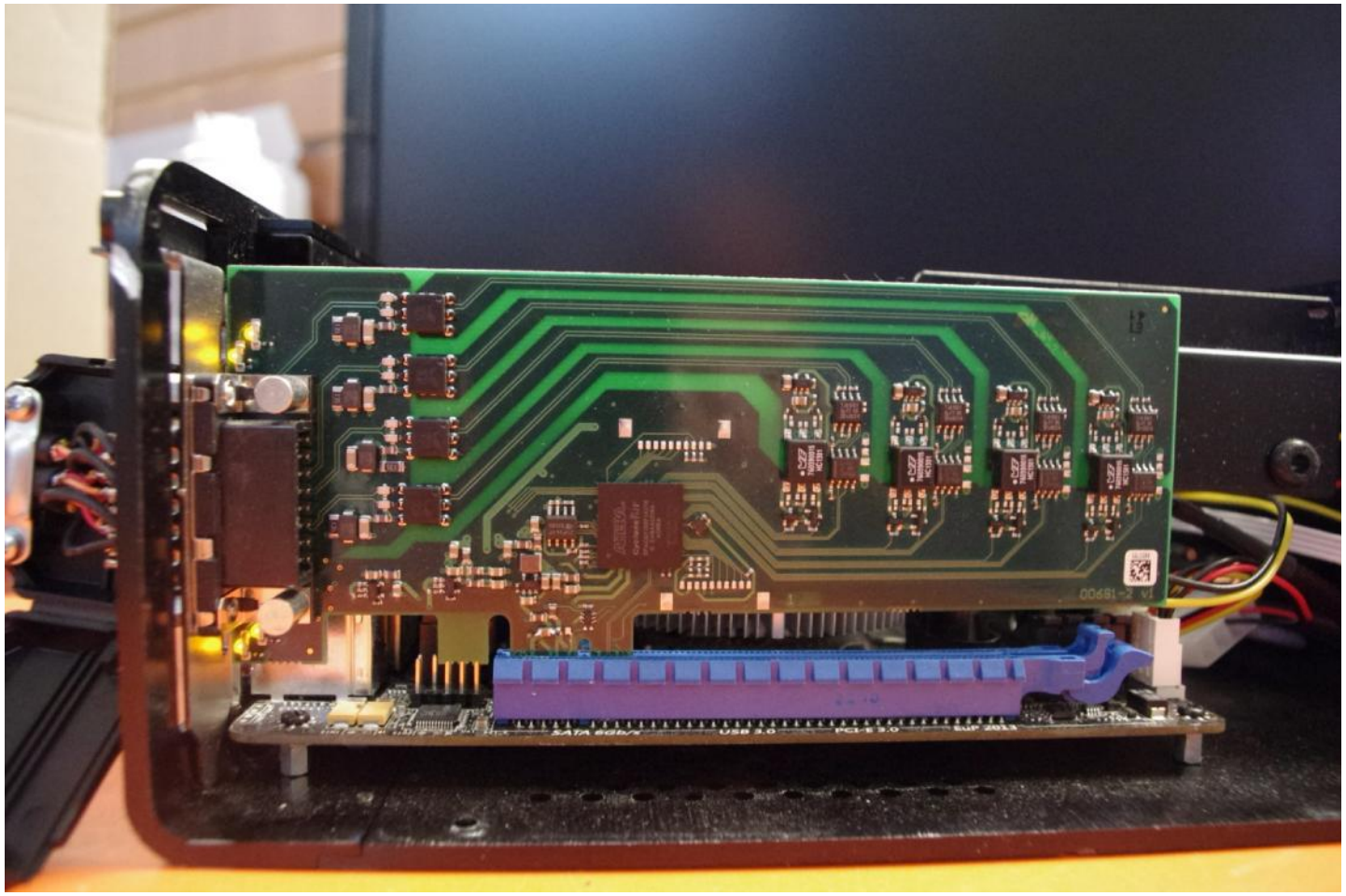
The test and verification Hardware



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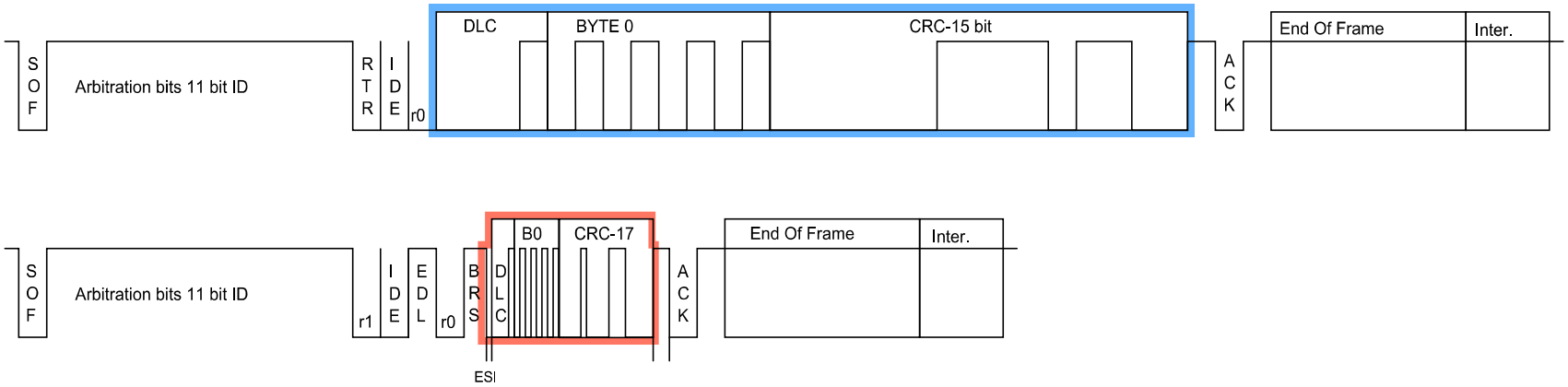
High Speed Data Phase



- 5x Bit Rate in Data Phase
- 1 Byte transmitted
- CAN work with 8 MHz sample at 1 Mbit/s
- CAN-FD work with 20 MHz sample at 5 Mbit/s
- CAN-FD is less demanding for the logic.

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Sample clock at different bit-rates

- The header show the bit definition for a typical bit.
- The value in the column is the necessary sample-clock for different bit-rates with this bit-definition.

Bit-rate Bit/s	CAN 8 Tq/ MHz	CAN 4 Tq/ MHz	CAN-FD 5 Tq/ MHz	CAN-FD 4 Tq/ MHz	CAN-FD 3 Tq/ MHz
62.5 k	0,500	0,250	0,312	0,250	0,187
125 k	1	0,500	0,625	0,500	0,375
250 k	2	1	1,250	1	0,750
500 k	4	2	2,500	2	1,500
1 M	**8**	4	5	4	3
2 M	16	8	10	8	6
3 M	--	--	15	12	**9**
4 M	--	--	20	16	12
5 M	--	--	25	20	15

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To use CAN-FD
is less complex compared to

Increase CAN bit-rate

- The only problem is modification of software to use more than 8 byte of data.

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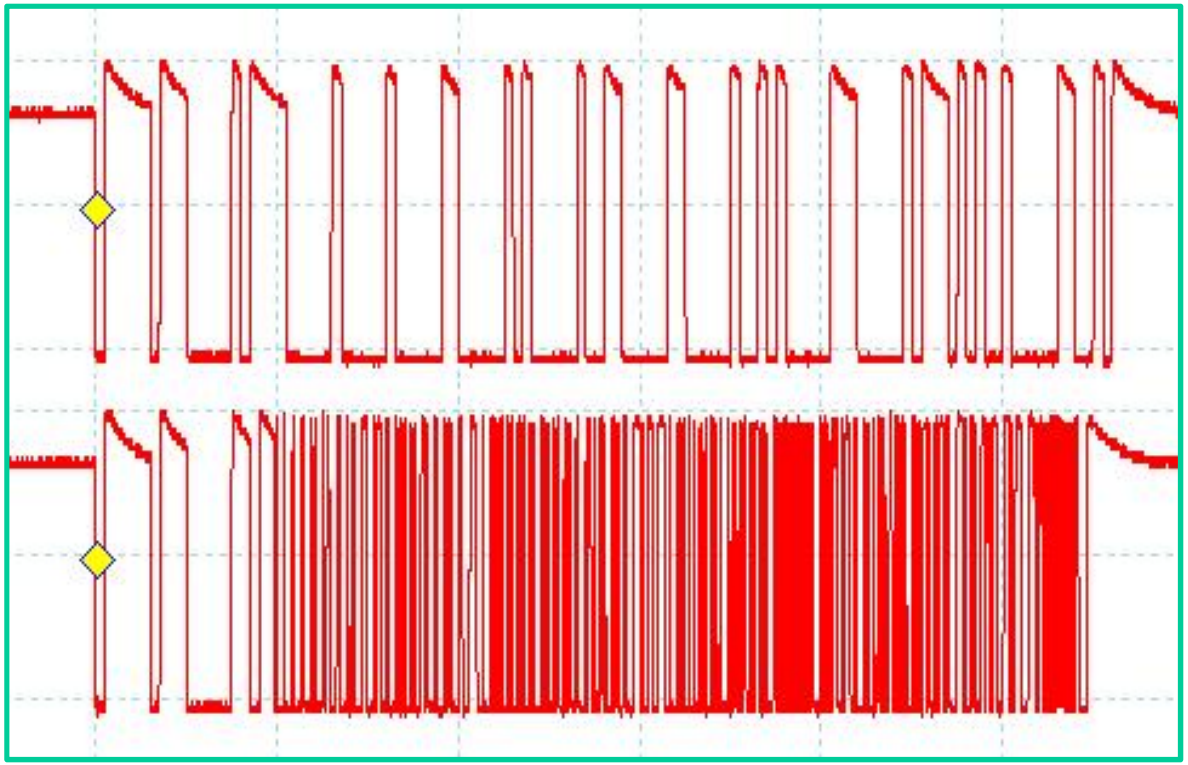
Side by side comparison

- Top graph is 8 Byte CAN at 0,5 Mbit/s.
- Lower graph is 64 byte at 4 Mbit/s. Shorter in time because CRC is shorter.



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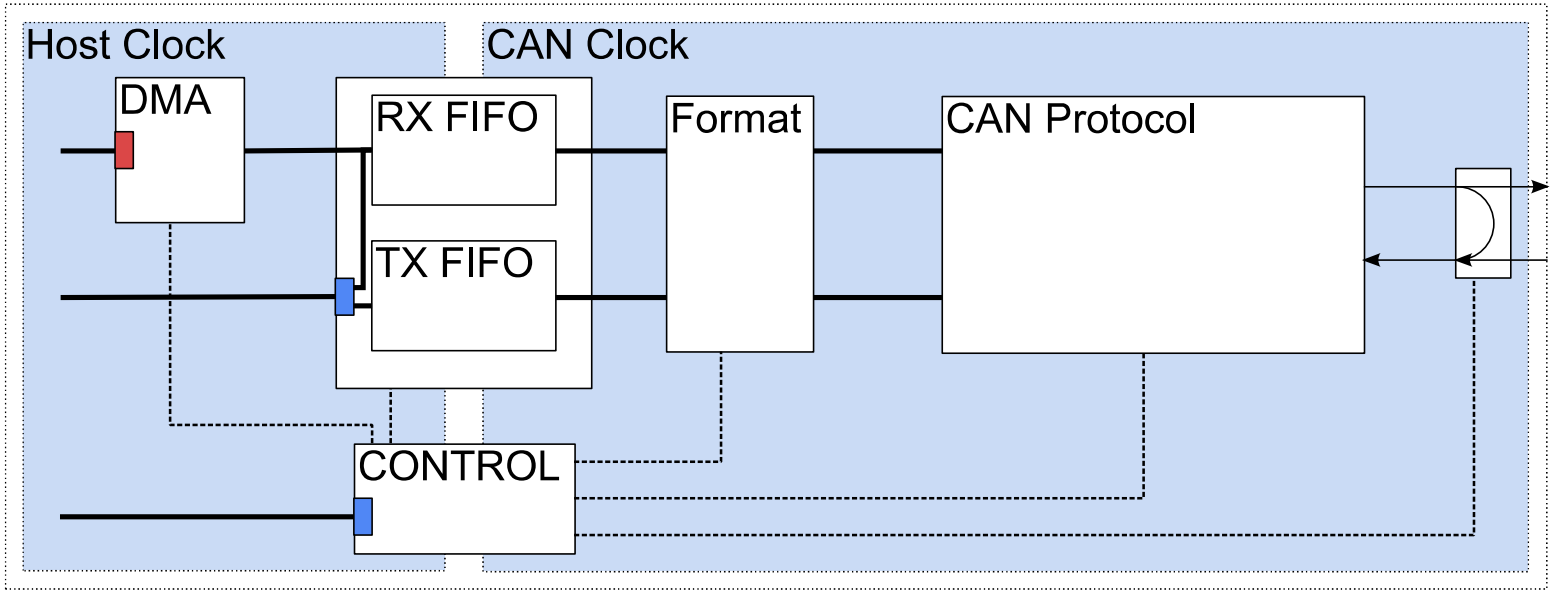
Block diagram over one, out of four, CAN-channels in the FPGA



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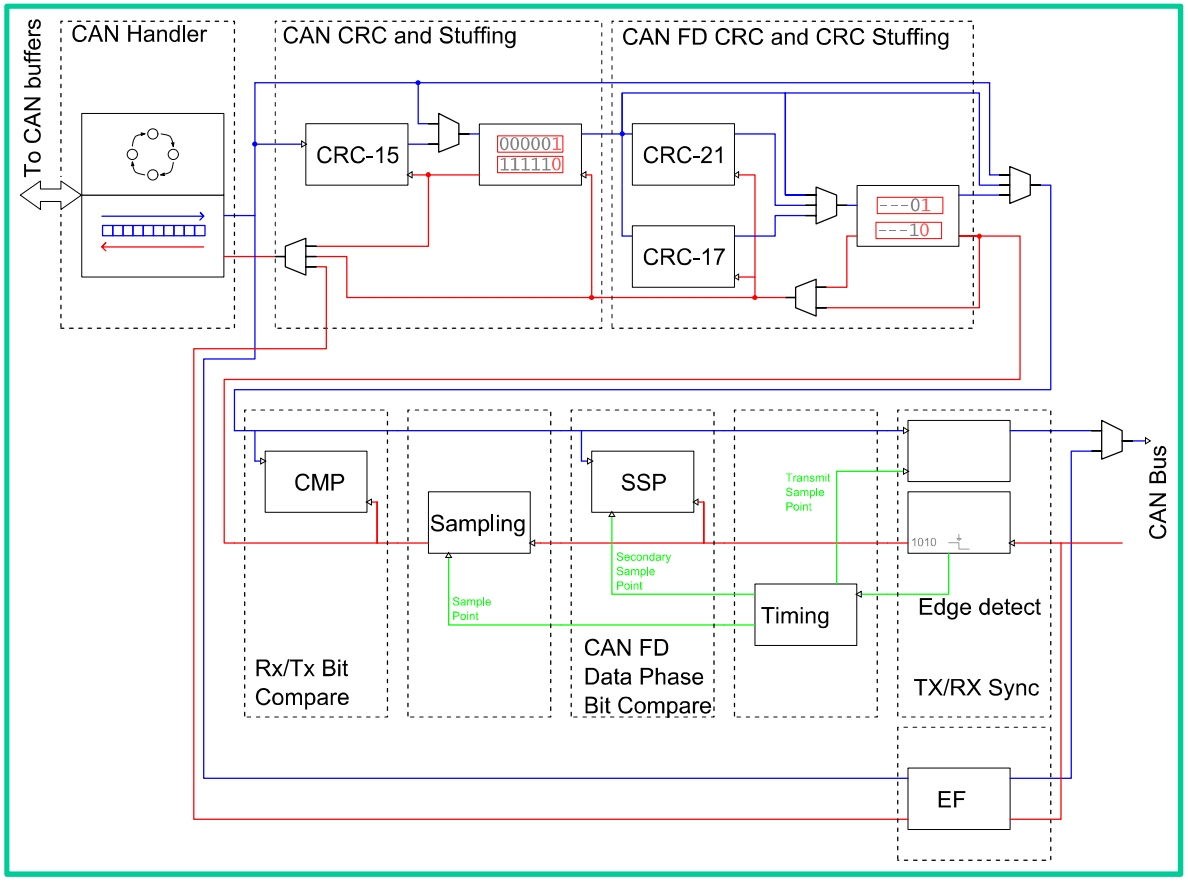
The bit-logic block

- Blue: TX-bit path
- Red: RX-bit path
- Green: High speed clock.



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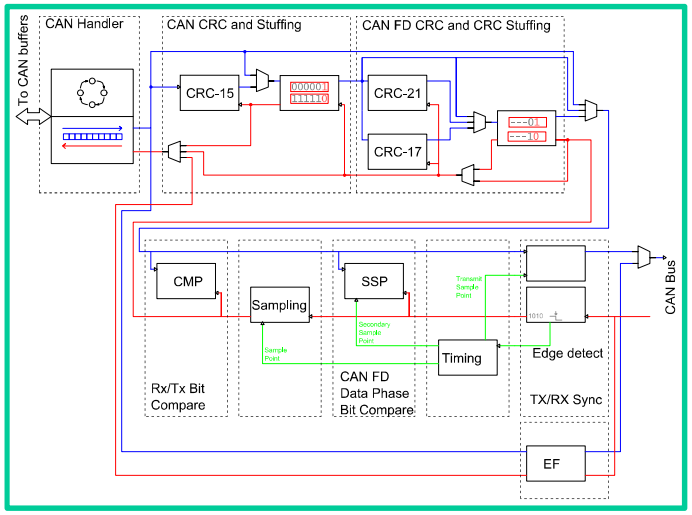
Logic added for CAN-FD

- CRC-17 and CRC-21
- Special Stuffing for the CRC-17, -21
- SSP, Secondary sample point
- No Error logic shown
- Extra control logic to select the correct bit path thru logic.



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Different DLC-coding

DLC	CAN Bytes	CAN-FD Bytes	CAN-FD CRC-
0-8	0-8	0-8	17
9	8	12	17
10	8	16	17
11	8	20	21
12	8	24	21
13	8	32	21
14	8	48	21
15	8	64	21

- Classic CAN will always have CRC-15.
- Remote Request in Classic CAN will always have 0 byte of data for any DLC.
- CAN-FD do have a different stuffing in the CRC-bits.

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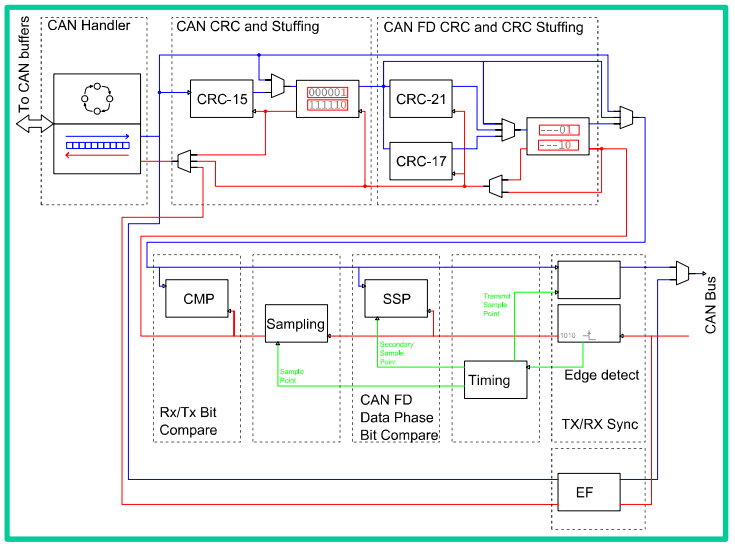
Different selections in the Logic

- 11-bit or 29-bit ID
- Use of DLC including remote request.
- Use of high bit-rate.
- Use of SSP.
- Use of CRC.
- Use of stuffing.



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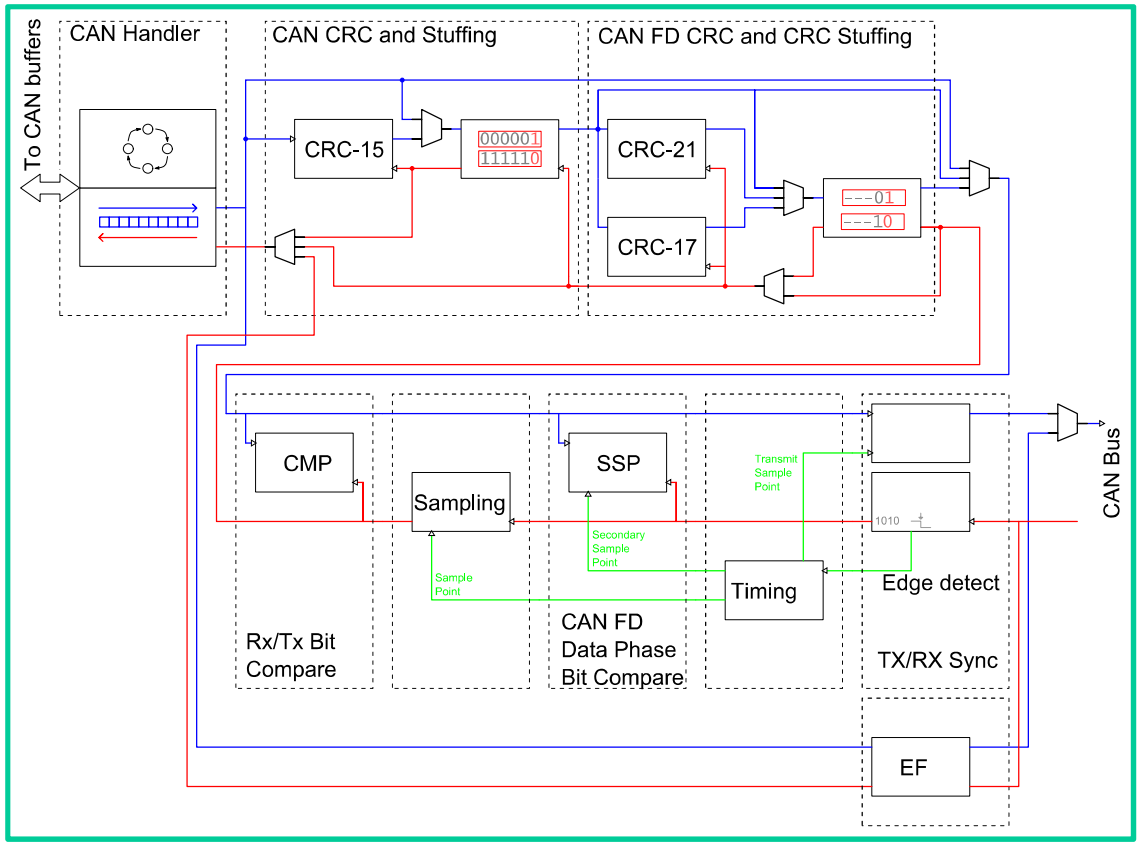
CRC and stuffing

- Classic CAN do stuffing after CRC-15
- CAN-FD do stuffing before CRC-17/21.
- CAN-FD have a special stuffing of CRC.



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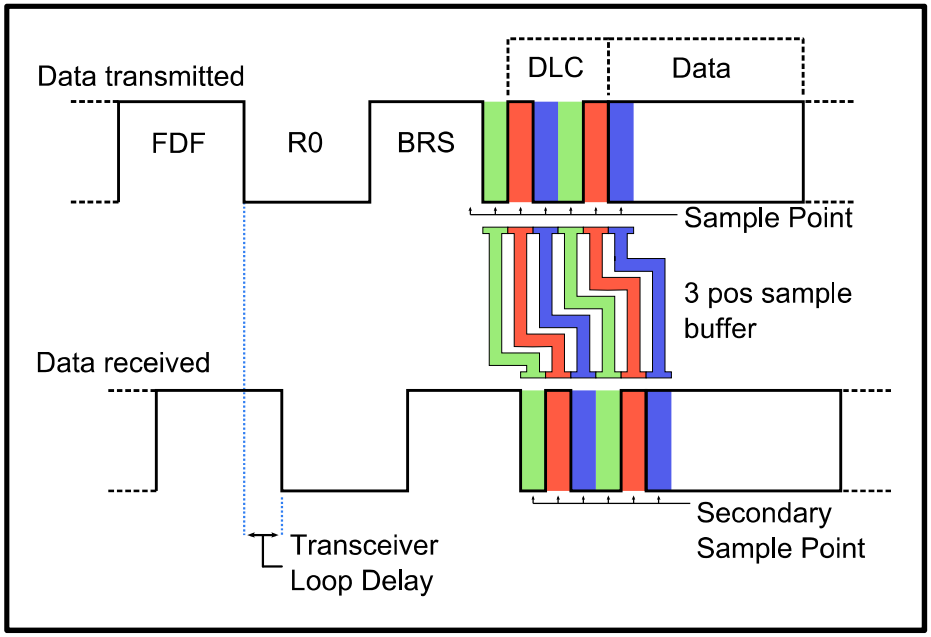
Secondary Sample Point, SSP

- Used for bit-error check when transmitting bits at data-rate.
- The loop delay from through transceiver is measured.
- The bit match will be delayed according to the measurement.



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Live demonstration of CAN-EF

- CAN Enhanced Format, CAN-EF.
- The intermediate step from CAN to CAN-FD.
- Can be mixed with Classic CAN and CAN-FD.

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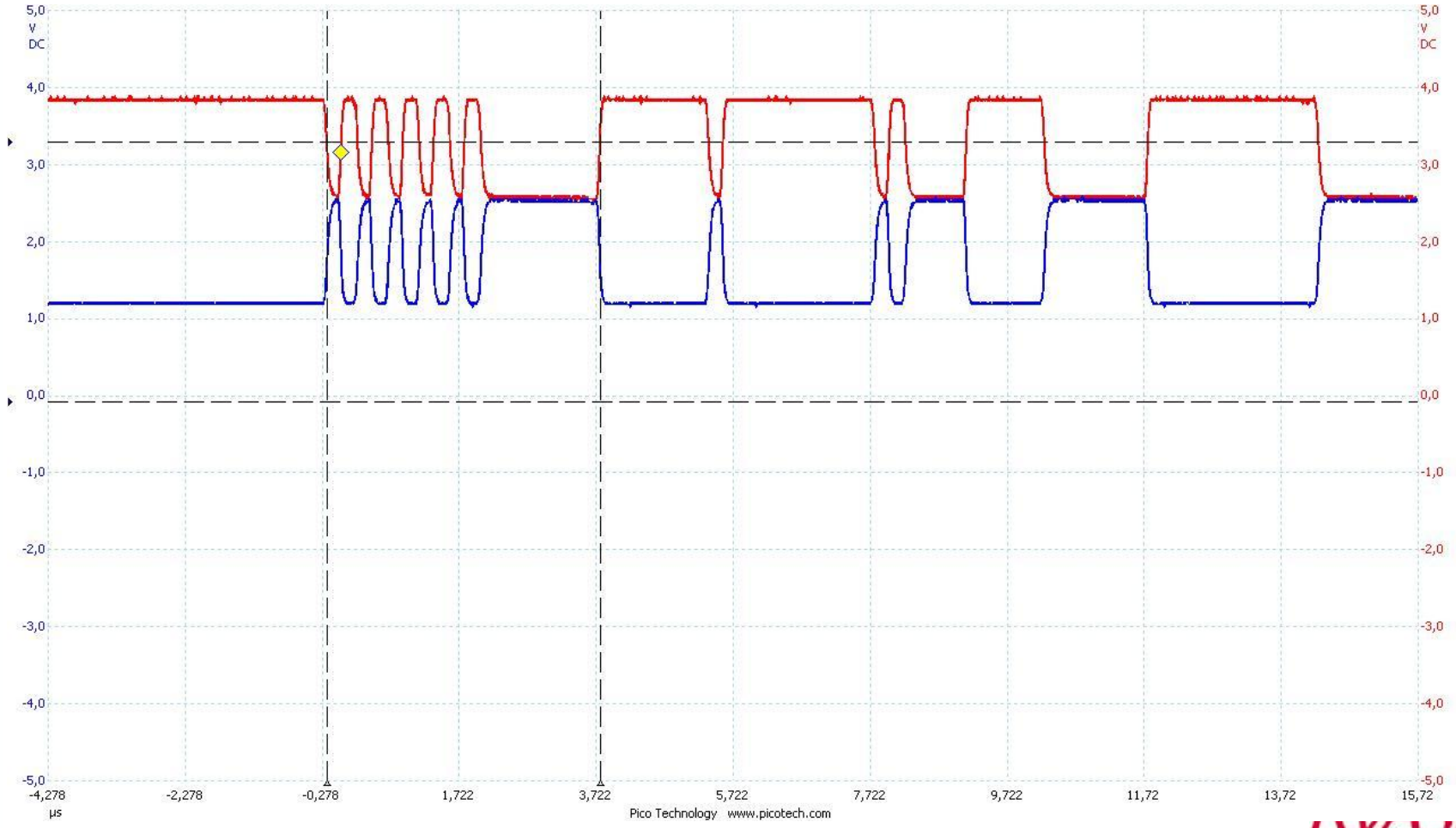
CAN-EF solution



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Why combine CAN-EF and CAN-FD?

- A step by step migration from Classic CAN to CAN-FD via CAN-EF.
- CAN-EF will increased band width within existing CAN-systems.
- CAN-EF improved CRC will cover also the Classic CAN-messages.
- Limited impact on CAN products available today.
- The diagnostic tools can stay with legacy bit-rates, only control applications running at higher CAN-EF bit-rates.
- CANopen can be unchanged still utilize higher band width CAN-EF.
- Limited impact on the silicon industry product portfolio.

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